

Atty. Docket No. OPP030889US
Serial No: 10/676,645

Amendments to the Claims

Please cancel Claims 6-7, add new Claims 21-34, and amend the remaining Claims as shown below.

Listing of Claims

1. (Currently Amended) A semiconductor device ~~having a pad formed by exposing a predetermined region of a metal line formed over a semiconductor substrate, the semiconductor device comprising:~~

a via over a semiconductor substrate;

a barrier metal layer on a surface of the via;

a metal line in the via over the barrier metal layer; and

an alloy layer formed on an upper surface of the metal line exposed through the pad,
wherein the alloy layer ~~is formed from a reaction by a heat treatment at a contacting surface between-~~ comprises a metal of the metal line and a low melting point metal having a melting point less than or equal to 1000°C.

2. (Currently Amended) The semiconductor device of claim 1, wherein the metal ~~line is made of~~ comprises copper.

3. (Original) The semiconductor device of claim 1, wherein the metal having the melting point less than or equal to 1000°C is selected from the group consisting of aluminum, lead, and silver.

4. (Currently Amended) The semiconductor device of claim 1, wherein ~~the a~~ thickness of the alloy layer is less than a thickness of the metal line.

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5. (Currently Amended) The semiconductor device of claim 1, wherein a protection layer made of ~~one of~~ silicon nitride ~~and or~~ silicon oxynitride is formed on the metal line except where the a pad is formed.

6. (Canceled)

7. (Canceled)

8. (Currently Amended) The semiconductor device of claim ~~[[6]]~~5, wherein a width of the pad is less than a width of the via.

9-20. (Previously Canceled)

21. (New) The semiconductor device of claim 1, wherein the pad is in a predetermined region of the metal line.

22. (New) The semiconductor device of claim 21, wherein a width of the pad is less than a width of the via.

23. (New) The semiconductor device of claim 1, wherein the barrier metal comprises a metal selected from a group consisting of Ti, Ta, TiN, and TaN.

24. (New) The semiconductor device of claim 1, wherein the barrier metal has a thickness between 200 and 800 Å.

25. (New) The semiconductor device of claim 1, wherein the alloy comprises a reaction product of the metal line and the low melting point metal.

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26. (New) The semiconductor device of claim 1, further comprising an insulation layer over the semiconductor device, wherein the via is within the insulation layer.

27. (New) The semiconductor device of claim 26, wherein the insulation layer comprises an oxide layer.

28. (New) The semiconductor device of claim 23, wherein the barrier metal layer prevents the diffusion of copper from the metal line into the substrate.

29. (New) The semiconductor device of claim 1, wherein the alloy layer is completely within the via.

30. (New) The semiconductor device of claim 1, wherein the barrier metal layer covers all surfaces of the via.

31. (New) The semiconductor device of claim 5, wherein the alloy layer is exposed through the pad.

32. (New) The semiconductor device of claim 1, wherein the barrier metal has a thickness of ~500 Å.

33. (New) The semiconductor device of claim 26, wherein a top surface of the alloy layer is lower than a top surface of the insulation layer.

34. (New) The semiconductor device of claim 1, wherein the barrier metal layer contacts the substrate.

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Amendments to the Figures

As requested by the Examiner during the interview of March 23, 2006, Figures 1A-1F have been amended to show a barrier metal layer 10 lining the surface of the via 100. Support for the barrier metal layer can be found in paragraphs [0006], [0008], [0010], and [0012] of the specification. Two Replacement Sheets (as required by 37 C.F.R. 1.121(d)) are attached to this Amendment.

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